IC-FEP-VPX3c

Xilinx Virtex®-7 3U VPX board with FMC Site

The **IC-FEP-VPX3c** expands our Front End Processing family with a solution based on **Xilinx Virtex-7 FPGAs** to respond to seemingly insatiable bandwith demand.

Designed for applications requiring a very high level of computing power in a compact 3U form factor, the **IC-FEP-VPX3c** board offers the highest bandwidth with the lowest power consumption.

The **IC-FEP-VPX3c** and the other building blocks of our 3U OpenVPX product ranges (Intel® and Freescale™ SBCs, Ethernet Switches & Routers, IO boards/FMC) running our Signal Processing Reference Design (including signal acquisition, Processing, DMA Engine, data storage, signal generation...) are the ideal platforms for customers who want to streamline development by concentrating their efforts on their most critical tasks.

RoHS 2002 / 95 / EC

Description

The Virtex®-7 FPGAs used on the **IC-FEP-VPX3c** are built on a high performance, low power 28nm process technology. This new design boosts I/O bandwidth, low-latency processing and global system performance.
The 7-Serie Unified Architecture also simplifies the process of migrating designs and IP from Virtex-6 and Spartan-6 FPGA families. Moreover, New designs can efficiently span the entire 7 series, including our Intel Core i7 boards with their embedded Kintex-7 FPGAs.

The Virtex®-7 FPGA interfaces with a flash for local storage of up to 3 bitstreams. It supports secured bitstreams and partial reconfiguration, further proving the versatility of the FPGA. A Clock tree allows synchronization from a unique clock selected between backplane REF_CLK+/-, from an FMC or a local oscillator.

The Fabric Links of the VPX backplane are connected to the FPGA GTX/GTH (FPGA dependent) transceivers, allowing data rate up to 13.1 Gbps.
The Embedded Hard IP Resources can be used to implement PCI Express Gen2/Gen3 (FPGA dependent) links, as well as the 10 Gigabit Ethernet ports (XAUI, 10GBase-KR).

The FMC site of the **IC-FEP-VPX3c** is compliant with the FPGA Mezzanine Card standard (VITA 57.1), allowing the installation of FMC modules provided by IC, third-party or developped by the customers.
Note however that FMC modules are equipped with high-performance I/O banks which support a maximum voltage of 1.8V. Any installed FMC modules must comply with this requirement (contact us for details).

As on all of our FMC sites, an optional I/O connector can route sixteen additional differential pairs from the FMC module directly to the P2 VPX connector.

Due to the modularity of the FPGA, the **IC-FEP-VPX3c** is compliant with several Module Profiles of the *OpenVPX* standard (TBD).

Main Features

Processing Unit
- Xilinx Virtex-7 XC7VX690T (other versionss on demand)
- Two banks of DDR3: 64-bit wide, 2GB each
- Optional QDRII+ 450MHz, 36-bit wide / up to 36 Mbits
- 128 MBytes of BPI NOR flash (bitstream storage)

VPX Interfaces
- Four 4-lanes fabric ports on P1
  - 16 GTX/GTH (Fat Pipes A, B, C & D)
- General purpose IOs on P2
  - 16 differential pairs (from FPGA)
  - 16 differential pairs (from FMC IOs connector)

FMC interfaces
- 8 GTX/GTH (FPGA part number dependent)
- 80 differential pairs
- 4 reference clocks

Miscellaneous
- PIC µ-controller for System Management to VITA 46.11
- 8 LEDs
- 8 configuration switches

Accessories
- Engineering kit : JTAG ports for direct FPGA configuration
- Rear Transition Module

The **IC-FEP-VPX3c** is a 3U VPX board compliant with 3U module definitions of the VITA 46.0 standard.

It is available in air-cooled (1") and conduction cooled (0.8") versions compliant with VITA 47 classes.

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XILINX Virtex-7 3U VPX board with FMC site

On-board firmware

The IC-FEP-VPX3c hardware platform is compatible with Xilinx development tools like VivadoTM and ISE Design Suite, Platform cable, etc.

Interface Concept provides :
►VHDL code for system services (DDR3, QDR, PCIe, Aurora, IC FMC interfaces, etc.) and reference designs such as PCIe DMA Engine, signal capture & processing, etc.
►Host drivers for our CPU (Linux, VxWorks)

Customers can implement their own real-time applications with the capability to integrate existing Open Source code or third-party IP cores.

Interface features

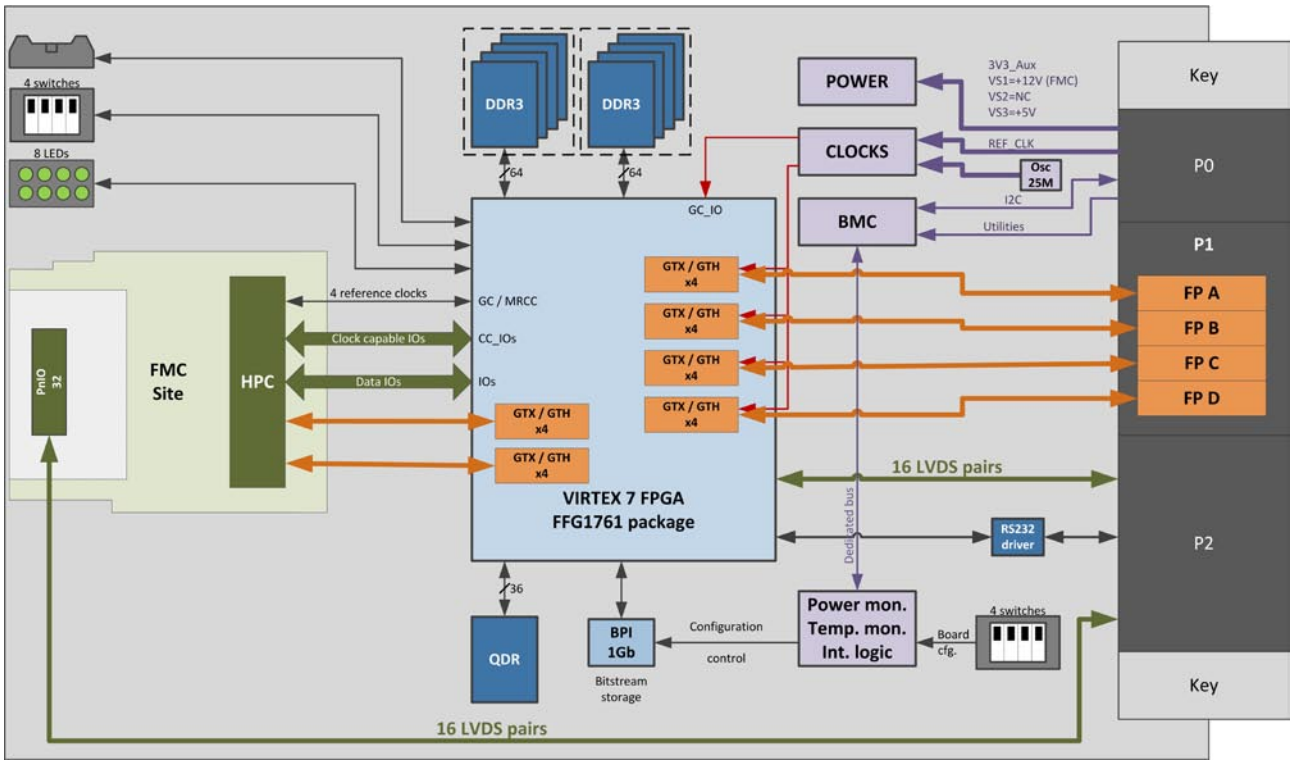
P0 connector
► VS3, 3V3_AUX, VS1 (+12V for FMC)
► REF_CLK
► I2C bus, utilities (SYSRESET, NVMRO, GAx)

P1 connector
► four 4-lanes fabric ports
• 16GTX/GTH(*) (ports A, B, C & D)
► RS232 (PIC µC)
► GPIOs - user defined

P2 connector
►General purpose I/O (on P2)
• 16 differential pairs
• 16 differential pairs (from optional FMC IOs connector)
► 1 RS232 (Virtex-7)
► 1 USB port (PIC µC)
► 2 SE GPIOs

FMC connector
► 8 GTX/GTH(*)
► 80 differential pairs
► 4 clocks (LVDS Diff)

Block Diagram



Environmental Specifications:

Please reference the **IC-FEP-VPX3c** page at **www.interfaceconcept.com**.

Ordering Information:

Please contact our sales department : tel. **+33 (0)2 98 57 30 30** - email : **info@interfaceconcept.com**

This document supersedes any earlier documentation relating to the products referred to herein. The information contained in this document is current at the date of publication. It may subsequently be updated or withdrawn without notice.

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