IC-FEP-TCAa

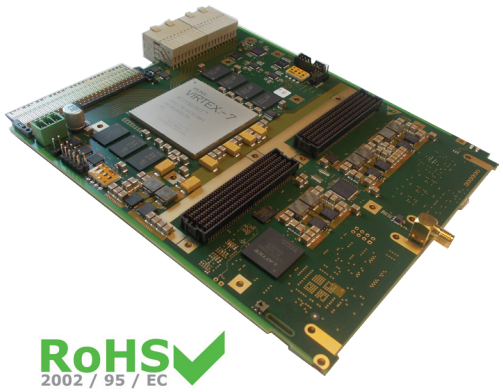
Virtex-7 MTCA.4 FPGA Processing Unit with two FMC

The **IC-FEP-TCAa** is a FPGA processing engine combining the high processing power of a Xilinx® Virtex-7™ with the substantial bandwith of the MTCA.4 form factor.

Designed for high performance Signal Processing applications, **IC-FEP-TCAa** is delivering the best that the current technology can provide. Its Virtex-7 FPGA features thirty six Serdes transceivers.

Two FMC (VITA 57.1) mezzanine sites allow the plugging of ADC, DAC, general IOs, sFPDP or additional FMC modules. In particular, IC has developed a four channels 1300MSPS 12 bit ADC FMC.

With this combination of high performance FPGA, dual FMC sites and high bandwidth MTCA.4 backplane, the **IC-FEP-TCAa** provides the best platform for very high demanding digital signal processing applications in particular in the High Energy Physics domain.



Description

The Virtex-7™ FPGAs used on the **IC-FEP-TCAa** are built on a state-of-the art, high performance, low power, 28 nm process technology.
Equipped with the Virtex-7™ VX690T (Speed Grade -2), the **IC-FEP-TCAa** provides the high performance logic (693K Logic Cells), high bandwith I/O with the GTH transceivers technology and high DSP resources (3600 DSP48E1 slices) requested by the most computation-intensive systems.

The two DDR3 memory banks supports a significant transfer data rate of 1600MT/s on two independant banks (Bank 1: 64b / 2GB, Bank2: 40b / 1.25GB).

The Fabric Links of the MTCA.4 backplane are connected to five FPGA 13.1Gb/s GTH transceivers, supporting: PCIe (Gen3), Aurora, (SRIO available thanks to specific IP). They are also connected to 38 LVDS running at more than 1 Gb/s.

The Virtex-7™ FPGA is interface with a SPI flash allowing the storage of three FPGA bitstreams (229 Mb bitstream size).

A Module Management Controller Unit based on the ATXMEGA128A1 of Atmel realizes IPMI interface, FPGA configuration and image management, on-board power, voltage and temperature monitoring.
Note: designed in cooperation with DESY in the Helmholtz Validierungsfond project «MTCA.4 for Industry» (HVF-0016).

Main features

Processor Unit
- One Xilinx Virtex-7 XC7VX690T(*) -2 or -3 offering
  - Two banks of DDR3: one 64 bit-wide and one 40 bit-wide
  - Three Quad SPI flash memory of 256 Mb each supported by iMPACT programming software for “Indirect SPI flash programming” operation

(*): XC7VX330T possible with MOQ

MTCA.4 Interfaces
- One PCIe x4 port
- 16 * Serdes lanes (two of them available for 1000 BASE-X ports - needs corresponding IP)
- 8 * M-LVDS for Trigger, Clock and Interlock
- Atmel Microcontroller for IPMI
- µRTM interface (I2C, JTAG, Interlocks, 38 * LVDS, 4 * Serdes, according to DESY Class D1.0-4 RevA.3)

FMC Interfaces (for each site from FPGA)
- 2 * GTH x 4 links
- 4 * clock differential signals
- 80 * LVDS

Front panel interfaces
- One USB

Accessories
- Engineering kit for debug : JTAG/COP, console,...
- Rear Transition Module

The **IC-FEP-TCAa** is available in air-cooled versions.

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Firmware

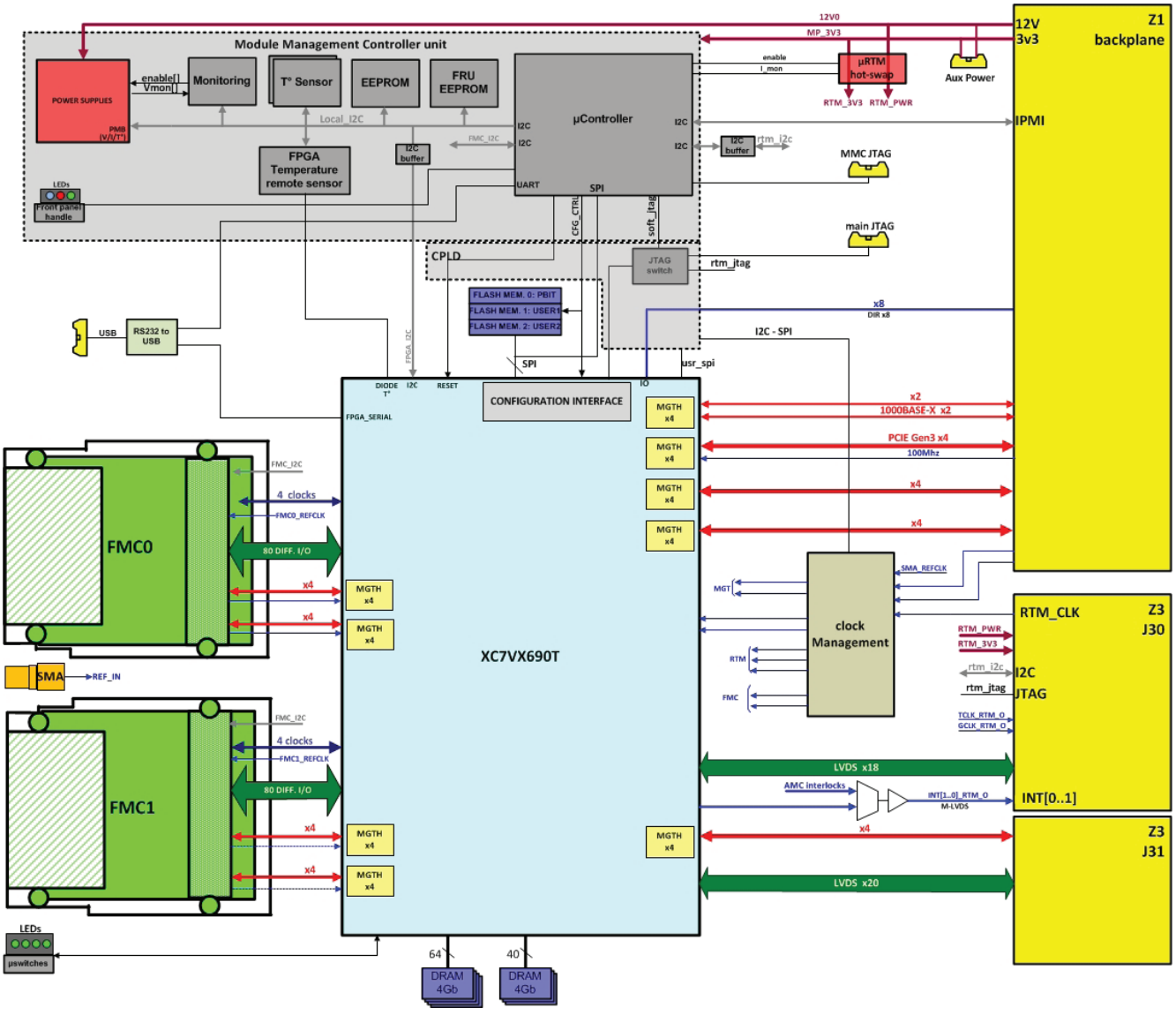
Management Controller Unit software MMC V1.0 for IPMI interface on the backplane, FMCs detection and start-up, µRTM power control including hot-swap, voltage and temperature monitoring, FPGA configuration management and management bus for µRTM (I2C).

The IC-FEP-TCAa hardware platform is compatible with Xilinx development tools like VivadoTM and ISE Design Suite, Platform cable, etc.

Interface Concept provides VHDL code for system services (PCIe, Aurora, IC FMC interfaces, etc.) and reference designs such as PCIe DMA Engine, signal capture & processing, etc.

Customers can implement their own real-time applications with the capability to integrate existing Open Source code or third-party IP cores.

Block Diagram



Environmental Specifications:

Please consult the **IC-FEP-TCAa** page at **www.interfaceconcept.com**.

Ordering Information:

Please contact our sales department : tel. **+33 (0)2 98 573 030** - email : **info@interfaceconcept.com**

This document supersedes any earlier documentation relating to the products referred to herein. The information contained in this document is current at the date of publication. It may subsequently be updated or withdrawn without notice.

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